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Continuous Benchmarking for a Massively Parallel Multi Physics Framework

Wednesday, March 6, 2024 1:50 PM (20 minutes)

waLBerla, an HPC software framework for multi-physics simulations based on the Lattice Boltzmann method, has consistently demonstrated exceptional parallel performance across various supercomputing platforms.

Maintaining a resilient codebase developed over a decade by multiple generations of developers is a paramount goal for waLBerla.
To achieve this, the framework has employed a continuous integration pipeline for a long time.
This pipeline ensures functional correctness and compatibility with a diverse array of compilers through systematic and automated testing.

Recognizing the importance of detecting performance regressions introduced by code changes, waLBerla has extended its continuous integration setup to include a continuous benchmarking pipeline.
Performance benchmarks run automatically on a range of CPU and GPU architectures, providing developers with swift feedback on how new commits impact the framework's performance.

In adapting to the dynamic landscape of HPC, waLBerla emphasizes versatility by testing on diverse hardware. This proactive approach not only ensures good performance but also provides developers with quick insights into the effects of their contributions.

Adhering to FAIR principles (Findable, Accessible, Interoperable, and Reusable), waLBerla stores profiling and timing data.
Developers benefit from an interactive visualization of this data, enabling them to discern performance trends over time.
This transparent approach empowers developers to make informed decisions within a performance-driven development process.

In summary, this presentation offers an in-depth exploration of waLBerla's comprehensive development infrastructure.
The delicate balance between functional correctness and performance optimization is achieved through a meticulous Continuous Integration Pipeline, a versatile Continuous Benchmarking Setup, and transparent, FAIR-compliant profiling and timing data visualization.
The audience will gain insights into how these elements collectively cultivate a development environment where waLBerla excels across diverse HPC landscapes.

Slot length

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