Proposal COST Action Neuromorphic Computing

for the Call 2025

Author: Researchers at Forschungszentrum Jülich

Research Coordination Objectives (RCOs)

1. Identify and prioritize key challenges in neuromorphic computing through reviews, expert input, and workshops, and define a roadmap for theory, hardware, and applications.
2. Promote synergies across neuroscience, hardware, AI, and HPC to align priorities, support sustainability, and foster interdisciplinary projects.
3. Develop and share best practices and benchmarks to enable validation across neuromorphic approaches, including metrics, datasets, and community tools.
4. Coordinate efforts across neuromorphic testbeds to support applications from real-time systems to scientific simulations and applied research.
5. Create a diverse application pool for neuromorphic computing, spanning sensor processing, healthcare, AI, robotics, and links to emerging technologies like quantum computing.

Capacity Building Objectives (CBOs)

1. Establish a pan-European network of researchers, industry, and stakeholders to connect neuroscience, devices, AI, and HPC, ensuring inclusive participation.
2. Develop training programs to equip researchers with cross-domain skills and access to platforms, infrastructure, and mentorship.
3. Raise awareness of ethical, policy, and dual-use issues through training and dialogue to support responsible innovation.
4. Foster exchange between academia, industry, and policy to align research with practical and market needs.
5. Support sustainability through early-career and industry collaboration, joint grant efforts, and long-term funding strategies.

Working Groups

WG 1: Foundations & Theoretical Models: Computational Neuroscience Concepts and Computational Limits	This WG focuses on the alignment between brain-inspired algorithms and neuromorphic hardware architectures. It explores how algorithmic models—such as learning rules (e.g., STDP, e-prop), reservoir computing, or ANN-to-SNN conversions (list is indicative)—can align with a variety of neuromorphic architectures. These may include digital event-based systems (e.g., Loihi, SpiNNaker), mixed-signal platforms (e.g., BrainScaleS), reconfigurable hardware (e.g., FPGAs), and emerging device concepts/architectures like in-memory computing. The examples given are indicative and not exhaustive, leaving room for additional contributions based on the interests of WG members. The focus is on understanding and improving how algorithm–architecture pairs interact in practice, including the role of encoding strategies, network topology, toolchain compatibility, and deployment workflows. As this alignment is typically mediated by software, tool support and abstraction layers also play an important role. The WG may also explore how

	HPC platforms can be used for simulating or prototyping neuromorphic algorithms, or how common software frameworks can support portability between neuromorphic and HPC systems. The WG provides a basis for sharing experience, identifying areas of difficulty, and jointly shaping methods and practices across the neuromorphic stack.
WG 2: Neuromorphic Devices & Circuits	This WG covers on the hardware side neuromorphic devices/materials (e.g., memristive devices, nanowire/dopant networks, oscillators, FeFETs) and small circuits made of these (e.g., LIF neurons using threshold switches) implementing memory and local learning. On the neuroscience side, it covers bio-inspired local learning mechanisms (e.g., biologically plausible backprop, predictive coding mechanisms). The WG should bring together experts from neuroscience and material science to discuss how neuroscientific learning/memory principles can be mapped on novel emerging devices and vice-versa how such devices can be tailored for local learning principles. This WG will have a strong link along the hierarchy towards neuromorphic computing architecture and algorithms.
WG 3: Neuromorphic Architectures & Brain-Inspired Algorithms	This WG covers neuromorphic hardware and architectures using novel emerging devices and brain-inspired algorithms coming from neuroscience. In this WG neuromorphic engineers and neuroscientist work together to map brain-inspired algorithms and circuitry motifs to existing and emerging neuromorphic chip architectures, identifying missing links in the process. The WG is linked to WG 1 on the device circuits and local learning at a lower hierarchy level and to WG 3 on use cases and benchmarking at a higher level.
WG 4: Applications & Use Cases, Evaluation & Benchmarking	This WG focuses on higher-level aspects of neuromorphic computing, such as identifying promising real-world application areas across domains (e.g., sensors, edge computing, multi-modal and multi-scale data analysis) and developing synthetic benchmarks and evaluation frameworks to support deployment on neuromorphic and HPC systems.
WG 5: Training, Education and Resource Pooling	The aim of this WG is to support the growth of the neuromorphic computing community by fostering interdisciplinary education and knowledge exchange. Key objectives include identifying relevant organizations and programs in the field, supporting the creation of educational tracks, and coordinating training initiatives across institutions. The WG will also work to promote resource and infrastructure sharing, and to build bridges across domains and expertise levels to strengthen collaboration and access.
WG 6: Dissemination & Outreach: Strategic	The aim of this WG is to communicate the outcomes of the Action effectively to scientific, industrial, and public audiences, including through strategic media and press

Coordination and Policy Alignment	engagement. It also seeks to foster stronger science communication practices, align outreach activities with EU policy priorities, and highlight funding opportunities relevant to the neuromorphic computing landscape. A further goal is to build bridges with industry stakeholders and policy makers, ensuring the Action has visibility and impact beyond the academic sphere.