NEST Conference 2025



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Type: Talk

Accelerated cortical microcircuit simulations on massively distributed memory

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Comprehensive simulation studies of dynamical regimes of cortical networks with realistic synaptic densities depend on compute systems capable of running such models significantly faster than biological real time. Since CPUs still are the primary target for established simulators, an inherent bottleneck caused by the von Neumann design is frequent memory access with minimal compute. Distributed memory architectures, popularized by the need for massively parallel and scalable processing for ML, offer an alternative.

We introduce extensible simulation technology for spiking networks on massively distributed memory using Graphcore's IPUs. We demonstrate the efficiency of the new technology based on simulations of the microcircuit model by (Potjans et al., 2014) commonly used as a reference benchmark. It represents 1~mm² of cortical tissue, and is considered a building block of cortical function. We present a custom communication algorithm especially suited for distributed and constrained memory environments, which allows a controlled trade-off between performance and memory usage. Our simulation code achieves an acceleration factor of 15x compared to real time for the full-scale cortical microcircuit model on the smallest device configuration capable of fitting the model in memory. This is competitive with the current record on a static FPGA cluster (Kauth et al., 2023), and further speedup can be achieved at the cost of lower precision.

With negligible compilation times, the simulation code can be be extended seamlessly to a wide range of synapse and neuron models, as well as structural plasticity, unlocking a new class of models for extensive parameter-space explorations in computational neuroscience.

Acknowledgements

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Preferred form of presentation

Talk (& optional poster)

Topic area

Simulator technology and performance

Keywords

microcircuit

Speaker time zone

UTC+1

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