Contribution ID: **145** Type: **Talk (15min + 5min)**

SUS: A new language for efficient Hardware Design

Tuesday 25 February 2025 16:20 (20 minutes)

SUS is a new HDL under development at the Paderborn Center for Parallel Computing. At its core, SUS is an RTL language intended to be used side-by-side with existing SystemVerilog and VHDL codebases. SUS has many interesting features, ranging from compile-time metaprogramming, to IDE information about clock domains and pipelining depths and metaprogramming debugging. Though this talk will mostly focus on the Latency Counting system of SUS. Latency Counting is SUS' approach to pipelining. People scoff at manual pipelining, but it is key to squeezing out the last bits of performance from resource-constrained hardware. Latency Counting relieves the mental burden of pipelining however, as it allows only local pipelining adjustments, and the compiler will - through the type system - adjust the surrounding hardware to handle the change.

I want to participate in the youngRSE prize

yes

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